ABSTRACT OF THE DISCLOSURE
INTERLEAVED PROCESSING SYSTEM FOR PROCESSING FRAMES
WITHIN A NETWORK ROUTER

A system and method for performing interleaved packet
processing in a network router. A packet to be routed
includes a source address bit pattern and a destination
address bit pattern that are each processed by a task
processor in accordance with a data tree. The data tree
includes multiple nodes linked by branches wherein an
instruction that is associated with each node within the
data tree is utilized for determining which branch is to be
taken in accordance with the source address bit pattern or
the destination address bit pattern. A first bank of
registers is utilized to load an instruction to be executed
by said task processor at each node of the data tree in
accordance with the source address bit pattern. A second
bank of registers is utilized for loading an instruction to
be executed by the task processor at each node of the data
tree in accordance with the destination address bit
pattern. A task scheduler enables the first bank of
registers to transfer an instruction loaded therein for
processing by the task processor only during even time
cycles and for enabling the second bank of registers to
transfer an instruction loaded therein for processing by
the task processor only during odd time cycles.